## REMARKS

In response to the rejections made on Claims 1-5 under U.S.C 102(b) as being anticipated by U.S Patent No. 5,655,099 Bjerge et al (Bjerge herein after) the applicant has provided the following response:

**The rejection of Claim 1 on Bjerge under 35 U.S.C. 102(b)**

In response to the rejection of claim 1, applicant has provided the following remarks pertaining to specific Examiner rejections. All remarks are fully supported through the existing specification without additional subject matter introduced.

In regards to the interrupt service routine, the Examiner has identified this as being equivalent to the access program taught by Bjerge. Applicant asserts however, that the interrupt service routine of the present invention differs from the access program of Bjerge. Bjerge teaches that "If a program placed in one bank has to activate programs or read/write data in another bank, it has to do this via an access program" (Col 1 lines 40-42). Simply put, the access program is a code segment specifically programmed to handle the switching of different memory banks for use by the processor (see Fig. 5). Furthermore, Bjerge teaches that the running program 30 in bank memory 15 "from time to time, requires the use of a subroutine function or task stored in bank memory 16" (Col 3 lines 58-59) and that the "running program 25 calls the access program 20" (Col 3 lines 29-30). Therefore, the access program is initiated by the running program in order to access a subroutine or data stored in a different bank memory.

This is in contrast to the present invention, as the hardware of the microprocessor initiates the interrupt service routine instead of the running program. It is generally known that interrupt service routines are directly initiated through an event such such as a user

input. Furthermore, an interrupt service routine is a programmable code segment that is executed only in response to this action. Bjerge states that the access program is specifically for switching memory banks for accessing programs or read/write data in other banks (see Fig. 5). Therefore, the access program of Bjerge is not customizable by a programmer of the microprocessor to automatically be executed in response to an interrupt such as a user or system interrupt. That is, the starting action of the access program of Bjerge must be specifically initiated in program code. Applicant further asserts that Bjerge does not teach the handling of an interrupt request, nor does he teach switching of the microprocessor to access the memory bank storing an interrupt service routine.

The recited limitation in Claim 1 is as follows: "storing an interrupt service routine in one of the memory banks" from part (a) and "when an interrupt occurs..." in part (b). Bjerge teaches storing an access program into ROM (Col 3 lines 20-25), which the applicant strongly asserts is fundamentally different from an interrupt service routine, and furthermore, does not describe the handling of an interrupt. Utilizing an interrupt service routine according to the present invention allows the author of the original program code to not have to be concerned with the switching of the memory banks because the interrupt service routine will handle this function automatically. Therefore, the interrupt service routine will pre-empt the original program code upon the interrupt and then return control to the original program after the memory banks have been switched.

For at least the reasons stated above, applicant asserts that the present invention differs from the teachings of Bjerge and kindly requests that the Examiner re-evaluate Claim 1 for its allowance.

**The rejection of Claims 2-5 on Bjerge under 35 U.S.C. 102(b)**

Regarding the rejections of Claims 2-5, please note that these claims are dependant on the currently amended independent Claim 1. Therefore, if Claim 1 is allowed, applicant asserts that Claims 2-5 be allowed as well as they are dependant on amended Claim 1.

**The introduction of new Claims 6-7**

Claims 6 and 7 were introduced in order to describe the present invention in terms of a hardware device structure. These Claims are fully supported through the existing specification without additional subject matter being introduced.

Claim 6 discloses a device comprising a microprocessor coupled to a memory unit, the microprocessor running a program code and switching memory banks of the memory unit in response to an interrupt to access the interrupt service routine, and reverting back to the program code upon execution of the interrupt service routine. Applicant asserts that Bjerge does not explicitly teach the automatic handling of an interrupt, and that the interrupt service routine of the present invention differs from the access program of Bjerge (please see remarks for Claim 1).

Claim 7 discloses the utilization of the stack for storing the program counter and bank number prior in response to the interrupt, prior to the switching of banks. This data is then popped back from the stack upon execution of the interrupt service routine in order to resume operation of the program code. As previously mentioned, this allows the author of the original program code to not have to be concerned with the switching of the memory banks because the interrupt service routine will handle this function automatically. Therefore, the interrupt service routine will pre-empt the original program code upon the interrupt and then return control to the original program after the memory banks have been switched.

Sincerely yours,

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